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Reducing the delay in conventional CSLA by using parallel path carry propagation SQRT CSLA Technique

S.Jakeer shareef[1], k.Jagadeesh kumar[2],Dr.V.Thrimurthulu[3]
[1]II M.Tech VLSI SD Student, CR Engineering College, Tirupathi, Chittoor (Dist) A.P, India,
[2] Asst.prof, ECE Dept., CR Engineering College, Tirupathi, Chittoor (Dist) A.P, India,
[3]Professor, Head of ECE Dept., CR Engineering College, Tirupathi, Chittoor (Dist) A.P, India,
[1]jakeer401@gmail.com, [2]jagadish.kasula@gmail.com, [3]vtmurthy.v@gmail.com

Abstract
The logic operations present in the conventional carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA are analyzed to study the data dependence and to identify redundant logic operations. By removing all these redundant logic operations involved in the conventional CSLA and proposed a new logical Technique. In the proposed Technique, the carry select (CS) operation is scheduled before the calculation of final-sum. Bit patterns of two opposite carry words (0 and 1) and constant c_{in} bits are used for logic optimization of CS and CG units. An efficient CSLA design is obtained using optimized logic units. The proposed CSLA design has a significantly less area and delay than the existing CSLA's. Due to the small carry-output delay, the proposed CSLA is a good design for SQRT CSLA. For different bit-widths.

I. INTRODUCTION

Area- efficient, high-performance and Low power VLSI systems are more used in small and mobile, portable devices, medical instrumentation, military applications, wireless receivers and many electronic devices. An adder is the main element of an AU. A complex processing DSP systems involves many numbers of adders. A best adder design essentially improves the speed of a complex DSP system. A ripple carry adder (RCA) uses a simple design, but carry propagation delay (CPD) is the main concern in this adder designing. Carry select and carry look-ahead methods have been suggested to reduce the CPD. A CSLA is a dual RCA. Configuration that generates a pair of sum words and output-carry words corresponding cin=0 and 1 and selects anyone out of each pair for final-sum and final carry output. A conventional CSLA has small CPD than an RCA, but the design is not efficient since it uses a RCA-RCA configuration. Few Times have been made to eliminate the dual use of RCA in CSLA. By used one RCA and one multiplexer (MUX) circuit instead of two RCA's.

The proposed a SQRT-CSLA to design large bit-width adders with small delay. In a SQRT CSLAs with increasing size are connected in a series manner. The main aim of this SQRT-CSLA structure is to given a "parallel path carry propagation" that helps to overcome the all adder delays. The BEC-based CSLA has a less logic resources than the conventional CSLA, but it has marginally higher delay. The common Boolean logic (CBL) based CSLA has a significantly. Less logic resource than the conventional CSLA but it has higher CPD, which is almost equal to that of the RCA. To reduce this problem, a CBL base SQRT-CSLA was proposed. However, the CBL-based SQRT-CSLA structure has a more logic resource and more delay than the BEC-based SQRT-CSLA. We observe that logic optimization mainly depends on availability of redundant logic operations. Whereas adder delay mainly depends on data dependence. In the existing structures, logic is optimized without taking any information from the data dependence. We made an analysis of this logic operations presented in the conventional and BEC-based CSLAs to study the data dependence and to identify redundant logic operations. Based on this identification, we have proposed a logical technique for the CSLA. The main contribution in this brief is logical technique is based on data dependence and optimized CG and CS units. Based on this technique, we have designed good logic design for CSLA. Due to optimized CG and CS units, the proposed CSLA has a significantly small ADP than the existing CSLAs.

II. RELATED WORK:

The rest of this brief is organized as follows. Basic operation of CSLA is presented in Section III. The proposed CSLA is presented in Section IV and the performance comparison is presented in Section V. The experiment results and discussion is present in section VI The conclusion is given in Section VII.

III. BASIC OPERATION

The logic operation of the n-bit RCA is operated in four stages:

1) Half-Sum Generation (HSG);
2) Full-Carry Generation (FCG);
3) Half-Sum Generation (HSG);
4) Full-Carry Generation (FCG).

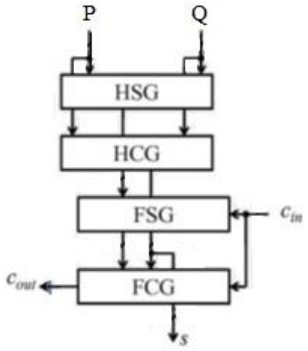

Fig.1: The logic operations of the RCA

The SCG unit requires most of the logic resources of CSLA and significantly contributes to the "critical path". Many numbers of logical structures have been suggested for good designing of the SCG unit. We made a study of the logic structures suggested for the SCG unit of conventional and BEC-based CSLAs. Ramkumar and H. M. Kittur, by suitable logic expressions. The main aim of this study is to detecting the redundant logic operations and data dependence. Therefore, we eliminating the all redundant logic operations and sequence logic operations based on their data dependence.

A. Conventional CSLA

The CSLA has two units:

1) The sum and carry selection unit (SCS)
2) The sum and carry generator unit (SCG)

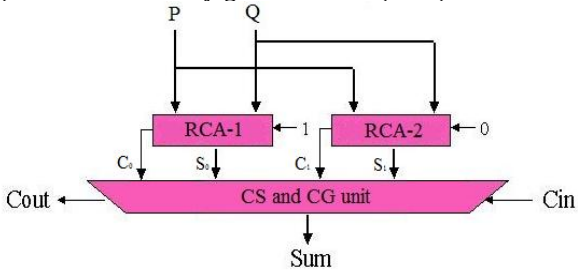

Fig.2: Conventional CSLA

As shown in Fig 2. The SCG unit of the conventional CSLA is consisting of two n-bit ripple carry adders, where n is the adder bit-width. Suppose two n-bit operands are added in the conventional CSLA, then RCA-1 and RCA-2 generate n-bit sum ($s^0$and s^1) and output carry (c^0out and c^1out) corresponding to input-carry (c_{in}= 0 and c_{in}= 1).

B. BEC-Based CSLA

As shown in Fig.3 the RCA calculates n-bit sum s^0_1 and c^0 out corresponding to c_{in}= 0. The BEC unit receives s^0_1 and c^0 out from the RCA and produce a (n + 1)-bit excess-1 code. The MSB of BEC represents c^1 out, in n LSBs represent s^1_1. We find that a significant amount of logic resource is spent for calculating $\{s^0_1, s^1_1\}$, and it is not a good approach to eliminate one sum-word after the calculation.

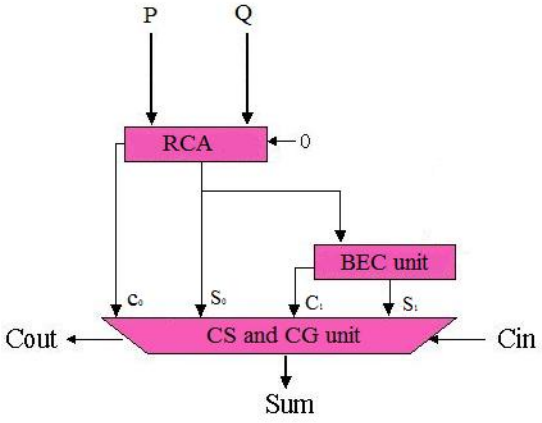

Fig.3: BEC-based CSLA

Instead, one can select the required carry word from the two opposite carry words $\{c^0$ and $c^1\}$ to calculate the final sum. The required carry word is added with the half-sum (s_0) to generate the final sum (s). Using this method, one can have three design advantages:

1) Calculation of s^0_1 is eliminated in the SCG unit.
2) The n-bit select unit is required instead of the (n + 1) bit.
3) Small output-carry delay.

IV. The proposed CSLA

The proposed system consists of:

1. HSG Unit
2. FSG Unit
3. CG Unit
4. CS Unit

The CG unit is Consisting of two CGs sub units (CG_0 and CG_1) corresponding to input carry '0' and '1'. The HSG receives two n-bit operands (A and B) and generate half-sum word (s_0) and half-carry word (c_0) of n-bits width each. Both CG_0 and CG_1 units receive s_0 and c_0 from the HSG unit and generate two n-bit full carry words c^0_1 and c^1_1 corresponding to input carry 0 and 1. The logic diagram of the HSG unit is shown in Fig 4.

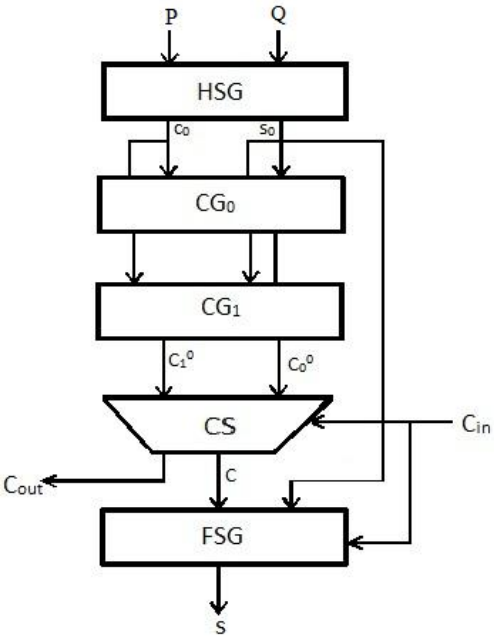

Fig.4: Proposed CSLA design,

The CS unit selects any one final carry word from the two carry words available at its input line using the control signal c_{in}. It selects c^0_1 when c_{in}=0; otherwise, it selects c^1_1 when c_{in}=1. The CS unit can be constructed using a 2-to-l multiplexer with different bit widths. However, we find from the truth table of the CS unit that carry words c^0_1 and c^1_1 follow a specific bit Patten.

V. PERFORMANCE COMPARISON

Estimation Method of Area and Delay:

We have considered all the gates to be made of AOI. A 2-input XOR is composed of one OR, two AND and two NOT gates. The delay and area of the 2-input AND, 2-input OR, and NOT gates are taken from the Synopsys Armenia Educational Department (SAED) 90-nm standard cell library datasheet for theoretical calculation. The delay and area of a design is calculated using the following relations:

$A = a \cdot N_a + r \cdot N_o + i \cdot N_i$

$T = n_a \cdot T_a + n_o \cdot T_o + n_i \cdot T_i$

Where (N_a, N_o, N_i) and (n_a, n_o, n_i), respectively, represent the (AND, OR, NOT) gate counts of the total design and its critical path. (a, r, i) and (T_a, T_o, T_i), respectively, represent the delay and area of one (AND, OR, NOT) gate. We have calculated the (AOI) gate counts of each design for delay and area estimation.

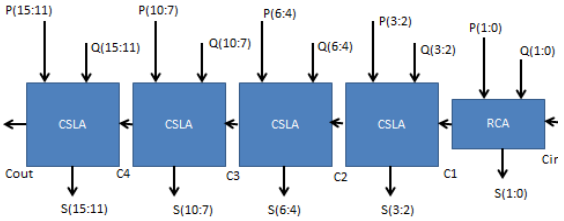

Fig.5: Proposed SQRT-CSLA

VI. EXPERIMENT RESULTS AND DISCUSSION

We have coded the SQRT-CSLA in VERILOG. Using this proposed CSLA structure and the existing CSLA structures also coded in different bit-widths of 16, 32, and 64. All the structures are simulated in the Xilinx ISIM (Integrated simulator) 9.2. And designs are synthesized in Xilinx XST (Xilinx synthesis tool), and finally generated bit-file is dumped in to a SPARTAN-3 FPGA BOARD for analysis. The synthesis result of Table, the proposed SQRT-CSLA present significantly less delay than the existing System.

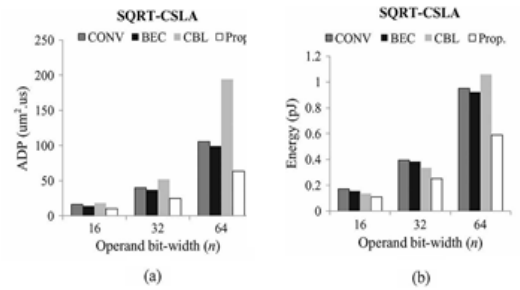

Fig.6: (a) Comparison of ADP (b) Comparison of energy consumption.

DESIGN	WIDTH (n)	DAT(ns)	POWER(uW)	AREA(um²)
CONVENTIONAL CSLA	16	5.61	30.5673	2890.52
	32	6.56	60.2573	6100.34
	64	8.37	113.6452	12613.2
BEC BASED CSLA	16	5.96	25.7958	2325.09
	32	7.64	50.0750	4801.33
	64	10.18	91.1774	9809.75
PROPOSED CSLA	16	5.55	19.6652	1813.45
	32	6.59	38.1886	3735.36
	64	8.35	70.6244	7603.89

Table: Comparison of different CSLA's

We can find from Fig.4 that the proposed SQRT-CSLA design offers a saving of 39% ADP and 37% energy than the RCA-based conventional SQRT-CSLA; 32% ADP and 33% energy than the BEC-based SQRT-CSLA and 55% ADP and 30% energy than the CBL-based SQRT-CSLA on average, for different bit-widths.

VII. CONCLUSION

We have studied the logic operations involved in the both CSLAs to study the data dependence and to identify redundant logic operations. We have removed all the redundant logic operations of the conventional CSLA and proposed a new logical technique for the CSLA. In the proposed Technique, the CS operation is scheduled before the calculation of final sum, which is different from the conventional CSLA. Carry words corresponding to input-carry '0' and '1 generated by the CSLA based on the proposed Technique follow a specific bit pattern, which is used for logic optimization of the CS unit. Constant input bits of the CG unit are also used for logic optimization. Based on this, optimized structures of CS and CG units are obtained. Using these optimized logic structures, a good structure is obtained for the proposed CSLA. The proposed CSLA design has a significantly less delay and area than the existing CSLA. Due to the small carry-output delay, the proposed CSLA structure is a best design for the SQRT-CSLA, for different bit-widths**.**

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AUTHORS:

S.Jakeer shareef received his B.Tech degree in Electronics & Communication Engineering from shree instuite of technical education, Tirupati (A.P), India, in the year 2013. Currently pursuing his M.Tech degree in VLSI System Design at Chadalawada Ramanamma Engineering College, Tirupati (A.P), India. His area of research Includes Low power VLSI design.

K.Jagadeesh Kumar Assistant Professor in ECE Dept. He received his Graduation in Electronics & Communication Engineering in GATE institute of technical engineering college, Anantapur, Post-Graduation M.Tech in Sri Kottam Tulasi Reddy Memorial College of Engineering, JNTU Hyderabad.

Dr.V.Thrimurthulu M.E., Ph.D. MIETE, MISTE Professor & Head of ECE Dept. He received his Graduation in Electronics & Communication Engineering AMIETE in 1994 from Institute of Electronics & Telecommunication Engineering, New Delhi, Post-Graduation in Engineering M.E specialization in Microwaves and Radar Engineering in the year Feb, 2003, from University College of Engineering, Osmania University, Hyderabad, and his Doctorate in philosophy Ph.D from central university in the year 2012. He has done research work on Ad-hoc networks.